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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/312,835	05/17/1999	SEUNG-HWAN MOON	06192.0070	3103

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McGuire Woods LLP
1750 Tysons Boulevard
Suite 1800
McLean, VA 22102

EXAMINER
KUMAR, SRILAKSHMI K

ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 06/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/312,835	MOON, SEUNG-HWAN	
	Examiner	Art Unit	
	Srilakshmi K. Kumar	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Misawa et al (US 5,811,837) in view of Garlepp et al (US 6,198,307).

As to independent claim 1, Misawa et al disclose a liquid crystal display system comprising, a liquid crystal display (Fig. 1) including a plurality of data lines (Fig. 1, items 26-28), a plurality of gate lines (Fig. 1, items 24 and 25) intersecting the data lines and a plurality of pixel electrodes (Fig. 1, items 32 and 33) arranged in a matrix type and each having a switch connected to one of the gate lines and one of the data lines (col. 4, lines 50-64); a gate driver (Fig. 1, item 21, col. 4, lines 35-40) for successively applying a gate voltage to the gate lines to turn on the switches; a data driver (Fig. 1, item 12, col. 4, lines 35-40) for applying a gray voltage, corresponding to image data signals to the data lines;

and a timing controller for sending both the image data signals and a shift clock signal to the data driver, with a first signal wire through which the shift clock signal is transmitted,

Misawa et al disclose clock signals which are 180 degrees out of phase as shown in Fig. 11, and col. 12 lines 13-34. Misawa et al does not disclose a timing controller. Garlepp et al disclose a timing controller in Fig. 9, item 15, and col. 7, lines 12-37. It would have been obvious to one of ordinary skill in the art to incorporate the timing controller of Garlepp et al into

that of Misawa et al as they both disclose clock signals for a liquid crystal display as Misawa et al would have a timing controller similar to that of Garlepp and also, the timing controller would have been outputting the timing signals.

and a second signal wire through which a first clock signal having a frequency equal to the shift clock signal but having a phase difference of 90 to 270 degrees transmitted to ground.

Misawa et al disclose a second signal wire through which a first clock signal having a frequency equal to the shift clock signal but having a phase difference of 90 to 270 degrees (Fig. 11, items 2 and 9, and col. 12, lines 13-34) Misawa et al does not disclose where the second signal wire is transmitted to ground. Garlepp et al disclose in Fig. 9, items CTMN, and col. 7, line 38-col. 8, line 4, where the second signal wire (CTMN) is connected to ground. It would have been obvious to one of ordinary skill in the art that this feature of the second signal wire connected to ground as shown by Garlepp could have been incorporated into that of Misawa et al as Misawa does not show where the end of the signal wire leads and thus could have been interpreted to be similar to that of Garlepp et al. The second signal wire connected to ground is advantageous as it enables the display to reduce noise.

As to independent claim 10, limitations of claim 1, and further comprising, a circuit board including a timing controller for generating a first image data signal and a second image data signal and generating a first shift clock signal and a second clock signal with a phase difference of 90 to 270 degrees that respectively shift the first image data signal and the second image data signal, a first image data signal wire and a second image data signal wire through which the first image data signal and the second image data signal are respectively transmitted (Fig. 13B), a data driver (Fig. 1, item 12) receiving the first image data signal and the second

image data signal and the first shift clock signal and the second shift clock signal from the timing controller (Fig. 1, items 32 & 35, col. 4, lines 36-col. 5, line 5) and applying a gray voltage corresponding to the first image data signal and the second image data signal to the data lines shown by col. 4, lines 36-col. 5, line 5.

As to dependent claim 2, limitation of claim 1, and further comprising wherein the second signal wire is connected to said ground through a predetermined resistance value. Misawa et al do not disclose where the second signal wire is connected to said ground through a predetermined resistance value. Garlepp et al disclose in Fig. 9, items CTMN, and col. 7, line 38-col. 8, line 4, where the second signal wire (CTMN) is connected through a resistor to ground. It would have been obvious to one of ordinary skill in the art that this feature of the second signal wire connected to ground through a resistor as shown by Garlepp could have been incorporated into that of Misawa et al as Misawa does not show where the end of the signal wire leads and thus could have been interpreted to be similar to that of Garlepp et al. The second signal wire connected to ground is advantageous as it enables the display to reduce noise.

As to dependent claim 3, limitations of claim 2, and further comprising, wherein the first clock signal is generated in the timing controller. Misawa et al does not disclose a timing controller. Garlepp et al disclose a timing controller in Fig. 9, item 15, and col. 7, lines 12-37. It would have been obvious to one of ordinary skill in the art to incorporate the timing controller of Garlepp et al into that of Misawa et al as they both disclose clock signals for a liquid crystal display as Misawa et al would have a timing controller similar to that of Garlepp and also, the timing controller would have been outputting the timing signals.

As to dependent claim 4, limitations of claim 2, and further comprising, wherein the first signal wire and the second signal wire are provided on a circuit board as shown by Fig. 3a-3b, 4a-4d.

As to dependent claims 5 and 6, limitations of claim 4, and further comprising wherein the circuit board is a multi-layered printed circuit board and the first signal wire and the second signal wire are formed in parallel on the same layer or wherein the circuit board is a multi-layered printed circuit board and the first signal wire and the second signal wire are formed on different layers. Although Misawa et al and Garlepp et al do not explicitly state the signal wires are on the same layer or a different layer, it is obvious to one of ordinary skill in the art that the signal wires could have either been on the same circuit board or different circuit boards as the active matrix LCD panels are usually multi layered. In col. 2, lines 10-37, Misawa et al disclose where the active matrix address mode liquid crystal displays employing TFTs are know to provide high image quality.

As to dependent claims 7, and 12-17, limitations of claims 1 and 10, and further comprising, wherein the first clock signal has a 180 degree phase difference from the shift clock as shown in Misawa et al Fig. 11, and col. 12 lines 13-34.

As to dependent claim 8, limitations of claim 7, and further comprising, wherein the data driver comprises a plurality of data driver integrated circuits for receiving the image data signals and the shift clock signal from the timing controller and applying the gray voltage corresponding to the image data signals to the data lines of the LCD panel as shown in Figs. 1, 2a-2e, col. 4, lines 36-64 and col. 5, lines 37-62.

As to dependent claim 9, limitations of claim 8, and further comprising wherein the data driver integrated circuits comprise a shift register (Fig. 8, item 163), a D/A converter receiving the image data signals stored in the shift register and converting the image data signals to a corresponding gray voltage and an output buffer for temporarily storing the gray voltage from the D/A converter and applying the voltage to the data lines of the liquid crystal display. Kihara et al disclose a sampling transistor circuit (Fig. 8, item 166) is shown to receive the image data signals which are stored in the shift register and convert the signals and apply the voltage to the data lines of the lcd as shown in col. 11, lines 1-22. It would have been obvious to one of ordinary skill in the art that the sampling transistor circuit performs the same functions as claimed above.

As to dependent claim 11, limitations of claim 10, and further comprising wherein the first data signals are odd image data signals, and the second image data signals are even image data signals. Although Misawa et al Garlepp et al do not explicitly state where the data image signals are separated into odd and even, it would have been obvious to one of ordinary skill in the art that is known in the art that the image data signals are usually separated into that of odd and even for increased quality of images.

Response to Arguments

3. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 308-9051, (for formal communications intended for entry)

Or:

(703) 308-6606 (for informal or draft communications, please label

"PROPOSED" or DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive,

Arlington, VA, Sixth Floor (Receptionist)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Srilakshmi K. Kumar whose telephone number is 703 306 5575. The examiner can normally be reached on 8:00 am to 5:30 pm alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven J. Saras can be reached on 703 305 9720. The fax phone numbers for the organization where this application or proceeding is assigned are 703 306-0377 for regular communications and 703 308 9051 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305 4700.

Srilakshmi K. Kumar
Examiner
Art Unit 2675

SKK
May 19, 2002

STEVEN SARAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600